REMARKS

In the Official Action mailed on **January 12, 2004** the examiner reviewed claims 1-24. Claim 1 was objected to because of informalities. Claims 1-24 were rejected under 35 U.S.C. 102(b) as being anticipated by Marcuello et al. (*Value Prediction for Speculative Multithreaded Architectures*, hereinafter "Marcuello (1)") and further by Marcuello et al. (*Speculative Multithreaded Processors*, incorporated by reference in Section 2 of *Value Prediction for Speculative Multithreaded Architectures*, hereinafter "Marcuello (2)").

Objections to the claims

Claim 1 was objected to because of informalities. Specifically, the limitation "the speculative thread" on line 8 does not have sufficient antecedent basis.

Applicant has amended claim 1 to provide antecedent basis. Applicant has also amended claim 23 to correct the same lack of antecedent basis. No new matter has been added.

Rejections under 35 U.S.C. §102(b)

Independent claims 1, 12, and 23 were rejected as being anticipated by Marcuello (1) and further by Marcuello (2). Applicant respectfully points out that Marcuello teaches speculative execution of **different iterations of loops** (see Marcuello (2), section 2, first paragraph). Additionally, Marcuello teaches that the instructions executed by the threads executing the different iterations of the loop are broadcast to each thread for **simultaneous execution of the identical instructions** (see Marcuello (2), section 2, third paragraph).

In contrast, the present invention can speculatively execute **methods, functions, or procedures** (see FIGs. 2B, 3, 12A and 12B and page 9, line 22 to page 10, line 27 and page 17, line 24 to page18, line 15 of the instant application).

Speculatively executing a method, a function, or a procedure is different from executing different iterations of loops because executing a method, a function, or a procedure requires execution of different instructions by each thread, while executing different iterations of loops involves executing the same instructions in each thread.

Because the threads in Marcuello execute the same instructions they can share the same instruction cache. This is illustrated in FIG. 1 of Marcuello (2), which shows the ICACHE being shared by three threads TU_0, TU_1, and TU_2. In contrast, threads in the present invention do not share code. Hence, the present invention must provide a separate instruction cache for each thread. See FIG. 1 of the instant application.

There is no suggestion within Marcuello (1) or Marcuello (2), either separately or in concert, which suggests speculatively executing a method, a function, or a procedure thereby requiring separate instruction caches for each thread.

Accordingly, Applicant has amended independent claims 1, 12, and 23 to clarify that the present invention speculatively executes subsequent code which includes a method, a function, or a procedure and also includes a separate instruction cache for each thread. These amendments find support in FIGs. 2B, 3, 12A and 12B, on page 9, line 22 to page 10, line 27, and on page 17, line 24 to page18, line 15 of the instant application.

Hence, Applicant respectfully submits that independent claims 1, 12, and 23 as presently amended are in condition for allowance. Applicant also submits that claims 2-11, which depend upon claim 1, claims 13-22, which depend upon claim 12, and claim 24, which depends upon claim 23, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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